A Novel Way of LTPS Model Extraction with Hysteresis and Transient Current Analysis †

Chen-Hao Kuo, Yung–Sheng Tsai*, Ching–Chieh Tseng*, Chee-Wai Lau*, Chun-Yen Liu*, Hannibal Wang**, Leon Huang**, Scott Lin**, You-Pang Wei**, and Po-Tsun Liu***

*** AU Optronics Corporation , Hsinchu, Taiwan R.O.C**

**** Legend Design Technology, Inc., California, US**

Abstract

Time-sampling measurements are used in this paper to build time dependent LTPS TFT current model. The device model that considers bias and time dependent threshold voltage (V_{th}) shift and mobility degradation is implemented in Eldo through GUDM for simulating a pixel circuit as an indicator of panel performance.

Author Keywords

time-sampling measurement, LTPS, V_{th} shift, mobility degradation, Eldo, GUDM, transient current.

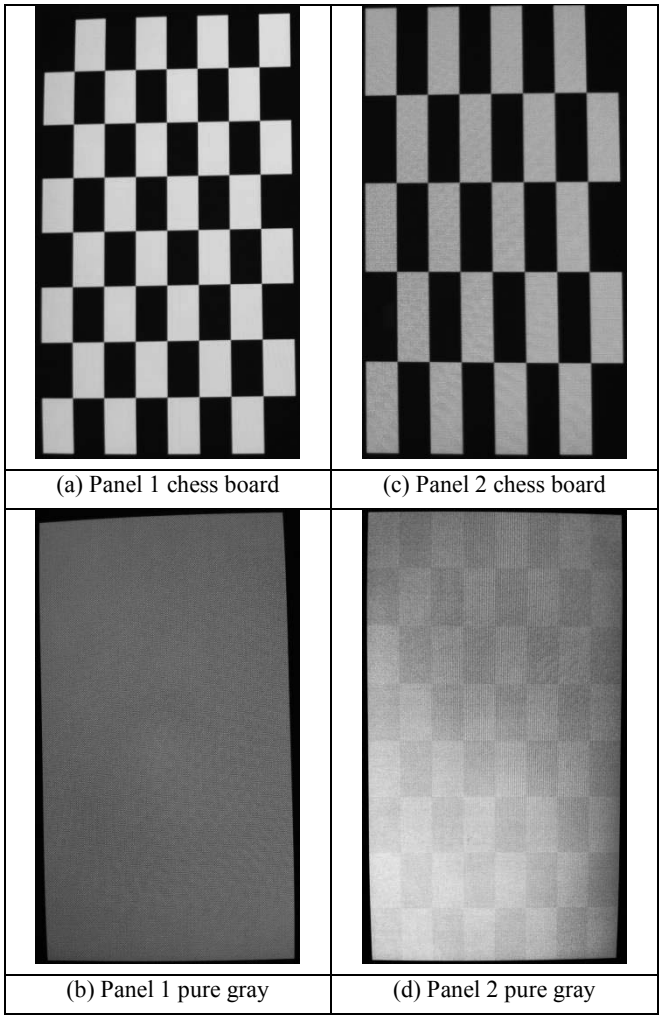
1. Objective and Background

The performance of a low-temperature poly-silicon (LTPS) thin film transistor (TFT) is usually judged by its threshold voltage (V_{th}), mobility (μ), sub-threshold swing (SS) and on-off current ratio (I_{on}/I_{off}) [1][2][3]. The roots of the variances on those performance indices are mainly the charge trapped in gate insulator layer, insulator -LTPS interface, grain-boundary and inside the grains [4][5]. The density of trap of each type can be derived with different kind of measures including hysteresis, SS and low-high frequency measure [6]-[10]. In addition to the trap concentration, the activation energy of the traps should be noticed too[11]. Nonetheless, the activation energy of the traps is bias dependent [11]. Therefore, the factors for threshold voltage shift include the gate and drain bias can be expressed as $\Delta V_{th} = \Delta V_{th}(V_{gs}, V_{ds}, \mathrm{Time}, \mathrm{Temp})$. Our goal is to extract the time and bias dependency factor of V_{th} shift from I_d-V_g and time sampling measure method. The objective of building this model is to enable designers to simulate the image retention time in AMOLED pixel circuit for panel performance estimation.

2. Results

A P-type LTPS TFT is fabricated with 120nm gate insulator layer and channel dimension of 30μm in length and 3 μm wide. The electrical characteristics were measured in ambient temperature (25℃).

When studying the image retention behavior, the chessboard pattern shown in Figure 1 is usually used to observe the image residual phenomenon which is the direct evidence of image retention and the criterion of the panels' quality check. The panel is controlled to display chessboard image for a certain length of time and then switch to pure gray image to observe how long the residual images of previous chessboard image remains. For the pixels, the image change consists of two types of operations, which are white (L255) to gray (L128) and black (L0) to gray (L128). Two panels with different image retention time are selected as the target for examining the effectiveness of the proposed model extraction method. One of them has residual image that lasts 10 seconds, and that of the other lasts 120 seconds. On each panel, one TEG is selected to represent the I-V characteristics of all TFT in the panel. In the following paragraphs, the origins of the residual image will be analyzed and an analytical approach of deriving and extracting the model parameters with transient current will be presented.



(a) Panel 1 chess board | (c) Panel 2 chess board

(b) Panel 1 pure gray | (d) Panel 2 pure gray

Figure 1. Residual image test samples

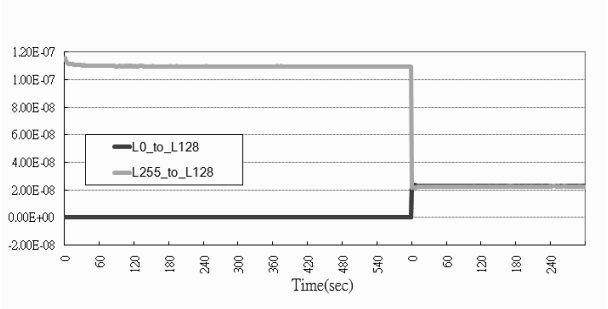
For an AMOLED panel, the luminance is from the OLED device whose current is controlled by the driving TFT. Therefore, we will focus on the variations of the LTPS TFT because the behavior variations of OLED are within milliseconds and is far from the scale of retention time observed [12]. To mimic the stability of the driving TFT current on a

panel, the TEGs on each panel are measured with different biases to provide similar current between the two TEGs with various luminance levels. The applied V_{ds} and V_{gs} biases at TEG 1 and 2 are listed in Table 1.

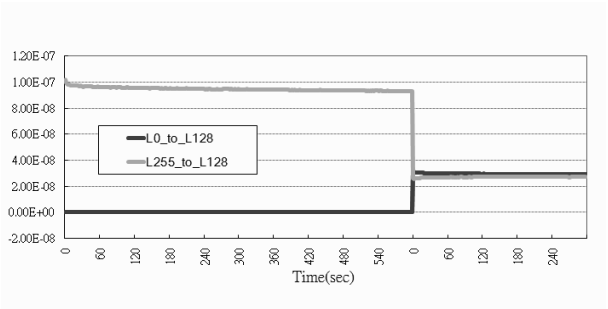
Table 1: Operating conditions for I_{ds} of driving TFT

	TEG 1		TEG 2	
	V_{ds}(V)	V_{gs}(V)	V_{ds}(V)	V_{gs}(V)
L255	-4.6	-1.4	-4.6	-1.8
L128	-4.6	-1.0	-4.6	-1.4
L0	-4.6	-0.2	-4.6	-0.2

After applying the biases to each TEG, the measured drain current of the TFT device under test is shown in Figure 2 where the green lines and pink lines are the measured currents with time during the operation of biasing condition changes from L255 to L128 and from L0 to L128, respectively. Ideally, when there is no stability issue in TFT, the current should be the same as soon as the bias voltage switches to the value for L128, independent of the bias that it was operated in. However, from the observation, TEG2 has an obvious difference between the green line and pink line after switching to L128. Nonetheless, when TFT operates in L255, both TEG current measures show a current drop at the beginning which is the result of charge trapping caused by high vertical electric field and the evidence of threshold voltage shift reported in previous researches [13][14].



(a) TEG1



(b) TEG2

Figure 2. Ids versus Time for (a) TEG 1 and (b) TEG 2

Based on previous literature, the time dependent threshold voltage shift (ΔV_{th}) is in agreement with stretched-exponential equation by the charge trapping mechanism and can be defined as $\Delta V_{th} = \Delta V_{th0} \cdot (1 - e^{-(t/\tau)^{\beta}})$, where ΔV_{th0} is the ΔV_{th} at infinite time, τ represents the characteristic trapping time constant, and β is the stretched-exponential exponent. ΔV_{th0}, that shows a strong dependence on bias stress, is mainly determined by the effective stress voltage and expressed as $\Delta V_{th0} \propto (V_{st} - V_{thi})^{\alpha}$, where V_{st} is the gate stress voltage, V_{thi} is the initial V_{th} and α is a parameter associated with the interface qualities. No matter which region the TFT is operated in, when the threshold voltage shift is relatively small comparing to V_{thi}, the time dependent drain current function ($I_{ds}(t)$) can be approximately expressed as

$$I_{ds}(t) \sim I_{ds}^{gray} + \Delta I_{ds} \cdot e^{-(t/\tau)^{\beta}}, \quad (1)$$

where I_{ds}^{gray} is the I_{ds} at infinite time with constant bias. At the moment that TFT operation enters L128, the difference between ideal and real current is

$$\Delta I_{ds} \propto (V_{gray} - (V_{thi} + \Delta V_{th0}^{gray})) \cdot \Delta V_{th0}^{gray}, \quad (2)$$

where V_{gray} is the voltage at L128 and ΔV_{th0}^{gray} is the L128 threshold voltage shift at infinite time. On the other hand, for operation from L255 to L128, the threshold voltage shift in L255 after a long time is defined as ΔV_{th0}^{white} which is usually larger than ΔV_{th0}^{gray} because of larger vertical electric field. The threshold voltage shift decreases from ΔV_{th0}^{white} to ΔV_{th0}^{gray} after operation changes from L255 to L128. This phenomenon is called quasi-trapping because the charges which were trapped during operation L255 are de-trapped (recovery) instead of trapping when TFT device is on. This recovered threshold voltage shift (ΔV_{th}) is in agreement with stretched-exponential equation either and can be expressed as

$$\Delta V_{th} = \Delta V'_{th0} \cdot e^{-(t/\tau')^{\beta'}} + \Delta V_{th0}^{gray} \quad (3)$$

where $\Delta V'_{th0} = \Delta V_{th0}^{white} - \Delta V_{th0}^{gray}$, τ' represents the recovered characteristic trapping time constant and β' is the stretched-exponential exponent. The time dependent current of TFT operating at L255 is similar to equation (1) but approaching the target value in different direction :

$$I_{ds}(t) \sim I_{ds}^{gray} - \Delta I'_{ds} \cdot e^{-(t/\tau')^{\beta'}}, \quad (4)$$

where I_{ds}^{gray} is the Ids at infinite time with constant bias, and $\Delta I'_{ds}$ as

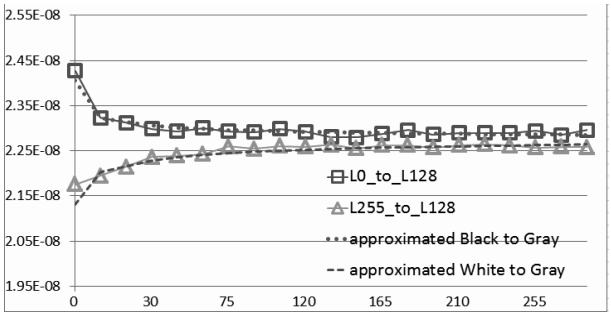
$$\Delta I'_{ds} \propto \left(V_{gray} - \left(V_{thi} + \Delta V_{th0}^{gray}\right)\right) \cdot \Delta V'_{th0}. \quad (5)$$

The measured transient current data are then used to extract the coefficients in trapping and quasi-trapping behaviors including τ, τ', β and β', whose values are listed in Table 2.

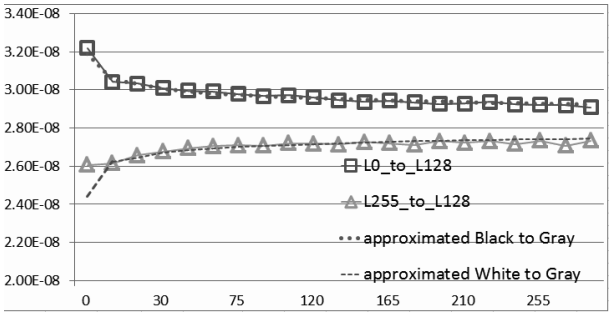
Table 2. Extracted coefficients for the driving TFT in trapping/quasi-trapping

	I_{ds}^{gray}	ΔI_{ds}	τ	β	$\Delta I'_{ds}$	τ'	β'
TEG 1	2.3e-8	1.3e-9	7	0.25	1.5e-9	20	0.35
TEG 2	2.8e-8	3.6e-9	100	0.28	3.9e-9	50	0.24

Figure 3 shows the measured transient current of both TEGs versus the calculated current with parameters in Table 2 and equations (1) to (5) which are perfectly matched with each other.



(a) TEG 1



(b) TEG 2

Figure 3. Measured and extracted transient current for (a) TEG1 and (b) TEG2

Although the non-ideality of TFT current can be explained with threshold voltage shift, it is not enough to explain the observation that we have on the panels because V_{th} variation, either from process variation or charge trapping, is usually compensated with circuits and controls [4][15][16], as what is included in the panels (e.g. 6T-1C pixel circuit) that we used for observation. And yet, residual images with different retention time are still commonly observable. Therefore, we need to introduce more factors to explain the image retention phenomenon in display panel beyond considering the V_{th} variation of TFT device. As explained in previous paragraphs, threshold voltage stability is caused by charge trapping, not only in gate insulator, but also in active layer too. When a charge is trapped in active layer, it affects the threshold voltage and mobility of the carrier simultaneous because the mobility is a function of gate bias, thermal voltage and threshold voltage [17]. The relation between effective saturation mobility (μ_{FET}) and the drain current of the TFT can be expressed as

$$\kappa \equiv \frac{\partial(\sqrt{I_{dsat}})}{\partial V_{gs}} \propto \sqrt{\mu_{FET}}, \qquad (6)$$

where I_{dsat} is the saturation drain current of TFT and κ is the mobility related coefficient. To understand the mobility variation after bias stress, we use a multi-cycle DC stress measurement method in which the device is repeatedly measured after stress with different voltage. To be exactly, the value of drain-source voltage is fixed at -4.6V and the gate-source voltages applied at the TEG is in a sequence with the order of L0, L0, L128, L128, L255, L255, L128 and L128 under 300 seconds for each. Since the conditions of these two TEGs are different, the operation of them in the designated level requires different voltages as listed in Table 3:

Table 3. Gate bias for multi-cycle DC stress measure

	L0	L0	L128	L128	L255	L255	L128	L128
TEG 1 (V)	-0.2	-0.2	-1.0	-1.0	-1.4	-1.4	-1.0	-1.0
TEG 2 (V)	-0.2	-0.2	-1.4	-1.4	-1.8	-1.8	-1.4	-1.4

With the bias change after each stress interval, the values of the mobility related coefficient κ for both TEGs are calculated by using equation (6) and listed in Table .

Table 4. Mobility factor κ under different stress conditions

	Initial	L0	L128_0	L255	L128_1	Delta L128
TEG 1	5.346e-04	5.345e-04	5.348e-04	5.352e-04	5.348e-04	-8.264e-09
TEG 2	4.725e-04	4.724e-04	4.731e-04	4.728e-04	4.727e-04	-4.732e-07

For each measure, although the stress conditions are different, the values of coefficient κ for L128 should eventually converge to the same value. Based on the equation (6) and Table 4, the mobility related coefficient κ is an important indicator for image retention behavior observation. According to the coefficient κ calculation results in Table 4, the value difference of κ between two L128 operations in TEG 1 is smaller than the one in TEG 2. As a result, the observed residual image of TEG 1 which is from panel 1 that has 10 retention time is smaller than that of TEG 2, the one from panel 2 whose retention time is longer than 120 seconds. The relation between mobility degradation and threshold voltage shift are obvious because when charges are trapped in active layer, carriers will have a harder time to move through and thereby a degradation of mobility is observed. The implementation of the coefficients to translate threshold voltage shift to mobility degradation is implemented in the model we have built but the discussion of it is left as future work to be done.

3. Impact

In this paper, we utilized transient-Id measure with selected gate-source biases to extract the coefficients for threshold voltage shift equation that explains the current degradation of panels without threshold voltage compensation. We also use the multi-cycle DC stressed Id-Vg to witness the mobility changes under different stress condition to explain the retention time difference in a panel that includes a threshold voltage compensation mechanism. The parameter extraction for threshold voltage shift equation and mobility degradation equation are provided by in the extraction tool TOME from Legend Design Technology Inc. The transient-Id measure and the serial DC stressed Id-Vg measure can be used at the same time for the extraction and building of the model. This model is then implemented by as a plug-in device through Mentor Graphics' GUDM and ELDO for simulating a 6T1C pixel to estimate the image retention time as an important indicator AMOLED panel performance, of which the discussion for the result will be left as a future work to follow.

4. References

[1] S. -D. Wang, W. -H. Lo, T. -Y. Chang, and T. -F. Lei, IEEE Elec. Dev. Lett., Vol. 26, No. 6, pp. 372-374, June, 2005.

[2] C.-H. Tu, T. –C. Chang, P. –T. Liu, H. –W. Zan, Y. –H. Tai, C. –Y. Yang, Y. –C. Wu, H. –Ch. Liu, W. –R. Chen, and C. –Y. Chang, Electrochemical and Solid-State Lett. 8 (9), G246-G248, 2005.

[3] T. Hirata, S. –I. Kuroki, M. Yamano, T. Sato, K. Kotani, T. Kikawa, 2014 21st International Workshop on Active-Matrix Flatpanel Displays and Devices (AM-FPD), July, 2014.

[4] C. –L. Fan, F. –P. Tseng, H. –L. Lai, B. –J. Sun, K. –C. Chiao, and Y. –C. Chen, International Journal of Photoenergy, Vol. 2013, Article ID 839301, 2013.

[5] Y. –M. Kim, K. –S. Jeong, H. –J. Yun, S. –D. Yang, S. –Y. Lee, H. –D. Lee, and G. –W. Lee, Electron Mater. Lett., Vol. 9(S), pp. 13-16, 2013.

[6] T-M. Pan et al., IEEE Electron Dev. Lett. 30, No. 1, 39–41 (2009).

[7] M. Kimura et al., Jpn. J. Appl. Phys. 40, No. 9A, 5227–5236 (2001).

[8] T. Noguchi, H. Hayashi, and T. Ohshima, Japan. J. Appl. Phys., vol. 25,p. L121, 1986.

[9] J. C. Liao, Y. K. Fang, C. H. Kao, and C. Y. Cheng, IEEE Electron Device Lett., VOL. 29, NO. 5, MAY 2008

[10] H-C Lin et al., J. Appl. Phys. Vol. 105, 054502 2009

[11] Y-M Kim et al., Journal of the SID 20/7, 2012 pp.355-359

[12] R. M. A. Dawson, Z. Shen, D. A. Furst, S. Connor, J. Hsu, M. G. Kane, R. G. Stewart, A. Ipri, C. N. King, P. J. Green, R. T. Flegal, S. Pearson,W. A. Barrow, E. Dickley, K. Ping, S. Robinson, C. W. Tang, S. Van Slyke, F. Chen, J. Shi, M. H. Lu and J. C. Sturm: Tech. Dig. IEDM (1998) p. 875.

[13] F. R. Libsch and J. Kanicki, Appl. Phys. Lett. Vol. 62, 1286, 1993.

[14] S. Zafar, A. Callegari, E. Gusev, and M. V. Fischetti, J. Appl. Phys. Vol. 93, No. 11, pp. 9298-9303, June, 2003.

[15] J. H. Lee,W. J. Nam, B. K. Kim, H. S. Choi, Y. M. Ha, and M. K. Han, IEEE Electron Device Lett., vol. 27, no. 10, pp. 830–833, Oct. 2006.

[16] C. L. Lin, K. W. Chou, F. C. Chang, and C. C. Hung, Solid-State Electronics 64 (2011) 10–13

[17] M. S. Shur, H. C. Slade, M. D. Jacunski, A. A. Owusu, and T. Ytterdal, J. Electrochem. Soc., Vol. 144, No. 8 2833, 1997